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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,679	12/29/2000	Anthony X. Jarvis	00-BN-067 (STMI01-00067)	9128

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,679	JARVIS ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005 and 03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-17,19-23 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-17 and 21-23* is/are rejected.

7)☒ Claim(s) *9,10,19,20 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 9-17, 19-23, and 25 have been considered. Claims 1, 5-7, 9-11, 15-17, 19-21, 23, and 25 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as filed 22 February 2005 and Amendment filed 03 March 2005.

Claim Objections

3. Claim 25 is objected to because of the following informalities: Please correct claim 25 from "The method as set forth in Claim 24" to --The method as set forth in Claim 21--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-4, 11, 13-14, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Divivier et al., U.S. patent Number 5,680,564 (herein referred to as Divivier) in view of Hull et al., U.S. Patent Number 5,922,065 (herein referred to as Hull) and in further view of Vondran, Jr., U.S. Patent Number 6,480,938 (herein referred to as Vondran).

6. Referring to claims 1, 11, and 21, taking claim 11 as exemplary, Divivier has taught a processing system comprising:

a. A data processor (Divivier Fig. 1) comprising:

i. An instruction execution pipeline comprising N processing stages (Divivier column 3, lines 22-23); and

ii. An instruction issue unit capable of fetching instructions into the instruction execution pipeline, the instructions fetched from an instruction cache (Divivier Figure 1, Element 16) associated with said data processor (Divivier column 4, lines 47-49), each of the fetched instructions comprising from one to S syllables (Divivier column 5, lines 1-4), the instruction issue unit comprising:

(1) A first buffer (Divivier Figure 1, Element 12) comprising S storage locations capable of receiving and storing the syllables associated with the fetched instructions,;

(2) A second buffer (Divivier Figure 1, Element 14) comprising S storage locations capable of receiving and storing the syllables associated with the fetched instructions; and

(3) A controller (Divivier Figure 1, Element 20 and column 3, lines 38-40) capable of:

(a) Determining if a first one of the storage locations in the first buffer is full (Divivier column 5, lines 40-51),

(b) In response to a determination that the first one of the storage locations is full, causing a corresponding

syllable in an incoming fetched instruction to be stored in a corresponding one of the storage locations in the second buffer (Divivier column 5, lines 40-51),

(c) In response to a determination that every syllable of one of the instructions has been stored in the first buffer, causing the syllables of the instruction to be transferred from the first buffer into at least one of a plurality of issue lanes leading into the instruction execution pipeline (Divivier column 3, lines 42-53).

iii. A memory coupled to said data processor (Divivier column 4, lines 47-49); and

iv. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (Divivier column 15, lines 35-39, which incorporates Shay, U.S. Patent Number 5,900,886, see Figure 1).

7. Divivier has not taught using a stop bit in a highest syllable of one of the instructions to determine whether every syllable of the instruction has been stored. However, Divivier teaches the use of variable length instructions (Divivier column 1, lines 60-65 and column 3, lines 15-20). Hull has taught a stop bit in a highest syllable of one of the instructions to determine whether every syllable of the instruction has been stored (Hull column 3, line 52 to column 4, line 20; and Figure 3). In regards to the position of the stop bit, it does not matter where the stop bit is located; shifting the

location of a part is not patentable subject matter (In re Japikse, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950); In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975)). A person of ordinary skill in the art at the time the invention was made would have recognized that the stop bit of Hull is necessary to determine where a variable length instruction ends, thereby ensuring that the correct instruction is executed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the stop bit of Hull in the device of Divivier to ensure correct execution.

8. In addition, Divivier has not taught wherein the instruction issue unit is capable of fetching syllables from multiple cache lines of the instruction cache during a single fetch. However, Divivier teaches the use of variable length instructions (Divivier column 1, lines 60-65 and column 3, lines 15-20). Vondran has taught variable length instructions (Vondran column 1, lines 14-25) and wherein the instruction issue unit is capable of fetching syllables from multiple cache lines of the instruction cache during a single fetch (Vondran column 2, lines 49-61; column 5, lines 40-66; column 15, lines 11-21; and Figure 1). A person of ordinary skill in the art at the time the invention was made, and as taught in Vondran, accessing more than one cache line in a single fetch improves cycle time and die area (Vondran column 1, lines 23-22). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate accessing multiple cache lines in a single fetch as taught by Vondran in the device of Divivier to improve die area and cycle time.

9. Claims 1 and 21 are nearly identical to claim 11. Claim 1 differs in its lack of a memory coupled to the data processor, and its lack of a plurality of memory-mapped peripheral circuits coupled to the data processor for performing selected functions in

association with said data processor, but encompasses the same scope as claim 11. Claim 21 differs in it being a method claim, but encompasses the same scope as claim 11. Therefore, claims 1 and 21 are rejected for the same reasons as claim 11.

10. Regarding claims 3 and 13, Divivier has taught wherein S=8 (Divivier column 3, lines 35-36).

11. Regarding claims 4, 14, and 22, Divivier has taught wherein S is a multiple of four (Divivier column 3, lines 35-36).

12. Regarding claims 8 and 18, Divivier has taught wherein said controller is capable of determining when all of the syllables in one of said fetched instructions are present in said first buffer, wherein said controller, in response to a determination that said all of said syllables are present, causes said all of said syllables to be transferred from said first buffer to said instruction execution pipeline (Divivier column 3, lines 28-32 and column 5, lines 1-16 and 35-52).

13. Regarding claims 10 and 20, Divivier has taught a switching circuit controlled by said controller and operable to transfer syllables from said second buffer to said first buffer (Divivier Figures 2 and 4 and column 5, lines 35-52).

14. Referring to claim 24, Divivier has taught wherein transferring at least one of the one to S syllables in the first buffer into the at least one of a plurality of issue lanes comprises (Divivier column 3, lines 42-53):

a. Determining when all of the syllables in one of the fetched instructions are present in the first buffer (Divivier column 3, lines 28-32 and column 5, lines 1-16 and 35-52); and

b. In response to a determination that all of the syllables are present, transferring all of the syllables from the first buffer to the instruction execution pipeline (Divivier column 3, lines 28-32 and column 5, lines 1-16 and 35-52).

15. Claims 2, 5-7, 12, 15-17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Divivier et al., U.S. patent Number 5,680,564 (herein referred to as Divivier) in view of Hull et al., U.S. Patent Number 5,922,065 (herein referred to as Hull) and in further view of Vondran, Jr., U.S. Patent Number 6,480,938 (herein referred to as Vondran).

16. Regarding claims 2 and 12, Divivier has taught wherein S=8, but has not explicitly taught wherein S=4. However, one of ordinary skill in the art would have recognized that decreasing the amount of usable syllables from 8 to 4 would not change the function of the processor, but would just decrease the number of usable syllables resulting in a scaling down of the hardware needed. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 4 syllables instead of 8 syllables (see In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976)).

17. Regarding claims 5 and 15, Divivier has taught wherein each of the syllables comprises 8 bits (1 byte), but has not explicitly taught where each one of the syllables comprises 32 bits. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 32 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 32 bit syllables instead of 8 bit syllables (see In re Rinehart, 531 F.2d

1048, 189 USPQ 143 (CCPA 1976), Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984,) and In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

18. Regarding claims 6 and 16, Divivier has taught wherein each of the syllables comprises 8 bits (1 byte), but has not explicitly taught where each one of the syllables comprises 16 bits. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 16 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 32 bit syllables instead of 8 bit syllables (see In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), Gardner v. TEC Systems, Inc, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), and In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

19. Regarding claims 7 and 17, Divivier has taught wherein each of the comprises 8 bits, but has not explicitly taught where each one of the syllables comprises 64 bits. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 64 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 32 bit syllables instead of 8 bit syllables (see In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), Gardner v. TEC Systems, Inc, 725 F.2d 1338, 220 USPQ 777 (Fed. Ck. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), and In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

20. Regarding claim 23, Divivier has taught wherein each of the syllables comprises 8 bits, but has not explicitly taught wherein each of the one to S syllables comprises one of: a) 16 bits, b) 32 bits, and c) 64 bits. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 16, 32, or 64 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 16, 32 or 64 bit syllables instead of 8 bit syllables (see In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), Gardner v. TEC Systems, Inc, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), and In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

Allowable Subject Matter

21. Claims 9-10, 19-20, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

22. Applicant's arguments with respect to claims 1-7, 9-17, 19-23, and 25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
13 May 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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